

# PLX6000 SERIES

## Low Noise Phase Locked Non-Integer Multiplier

### Features:

- Rugged Design
- Low Noise
- Lock Indicator
- Proven Technology
- Custom Designed to your exact requirement

### Applications:

- Coherent Local Oscillator
- Test Equipment
- Up/Down Converters



### Specifications:

Output Frequencies:	40 MHz to 1.0 GHz
Output Level:	+10 dBm min
Input Frequencies:	5.0 or 10.0 MHz
Input Level:	0 dBm $\pm$ 3 dB
Harmonics:	-40 dBc
Coherent Spurious:	-60 dBc
Non Coherent Spurious:	-90 dBc
Phase Noise:	See graph below
Operating Temperature:	0° C to +50° C
Lock Indicator:	TTL High=Locked
Supply Voltage:	+15 VDC $\pm$ 2% @ approx. 85 ma +5 VDC $\pm$ 2% @ approx. 100 ma
Connectors:	SMA (F) (Input Reference & RF Output) Filtercon (DC)
Size:	See outline drawing

The PLX6000 Series of phase locked multipliers are designed to achieve a fractional input to output multiplication relationship. This is accomplished by division and/or multiplication to maintain a coherence with the reference frequency; low noise performance is maintained throughout this process. Since frequency synthesis is used, the output signal does not have a direct ( $20 \log N$ ) noise relationship to the input signal. The technique provides precise control of the loop bandwidth thereby resulting in excellent noise performance and high suppression of undesired signals.

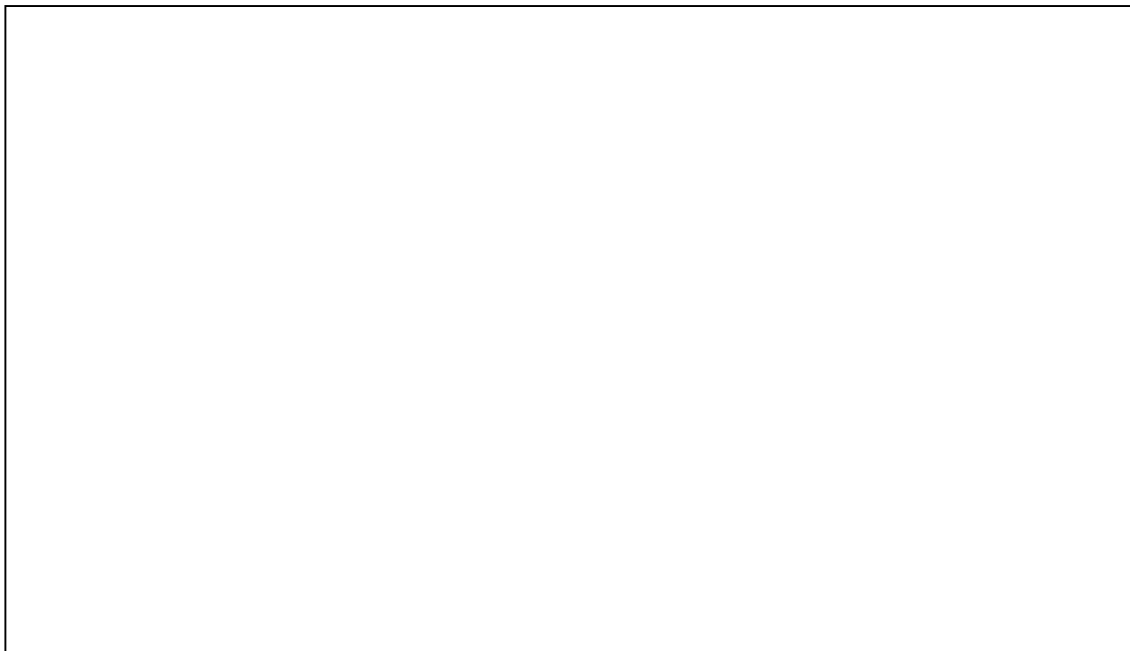
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## PLX6000 SERIES PHASE NOISE



## PLX6000 OUTLINE DRAWING



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